CLAIMS

I claim:

1. A method for generating a premodulation-filtered modulation waveform for transmitting octal symbols, the modulation waveform comprising a real part and an imaginary part comprising:

inputting to a logic unit successive octal data symbols, each comprising first , second and third information bits;

forming in said logic unit a first derived bit by combining the first and third information bits and a second derived bit by combining the second and third information bits;

forming first, second, third and fourth address bit sequences by collecting successive first information bits, second information bits, first derived information bits, and second derived bits respectively in corresponding registers;

generating first, second, third, and fourth filtered waveform segments based on said first, second, third, and fourth bit sequences;

combining the first and third filtered waveform segments to obtain a segment of said imaginary part of said modulation waveform; and

combining the second and fourth filtered waveform segments to obtain a segment of said real part of said modulation waveform.

2. The method of claim 1 in which said logic unit forms said first derived bit by an exclusive OR operation on said first and third information bits.

3. The method of claim 1 in which the logic unit forms the second derived bit by an exclusive OR operation on the second and third information bits and complementing the result.

4. The method of claim 1 in which the filtered waveform segments are represented by a plurality of numerical samples spaced over each symbol period.

5. The method of claim 1 in which the filtered waveform segments are represented by a sequence of sigma-delta values.

6. The method of claim 5 in which the filtered waveform segments are produced as a balanced signal represented on two outputs and are represented by a sequence of sigma-delta values and its complement.

7. The method of claim 1 in which the modulation waveform is generated in balanced form on two outputs for each of the real and imaginary parts.

8. The method of claim 1 in which combining first and third filtered waveform segments comprises forming a weighted sum of one or more numerical samples of the first filtered waveform segment with corresponding numerical samples of the third filtered waveform segment.

9. The method of claim 1 in which combining second and fourth filtered waveform segments comprises forming a weighted sum of one or more numerical samples of the second filtered waveform segment with corresponding numerical samples of the fourth filtered waveform segment.

10. The method of claim 1 in which combining first and third filtered waveform segments comprises connecting the first filtered waveform segment through a first impedance to an output terminal and connecting the third filtered waveform segment through a second impedance to said output terminal to produce a weighted sum of the combined first and third filtered waveform segments at said output terminal.

11. The method of claim 1 in which combining second and fourth filtered waveform segments comprises connecting the second filtered waveform segment through a first impedance to an output terminal and connecting the fourth filtered waveform segment through a second impedance to said output terminal to produce a weighted sum of the combined second and fourth filtered waveform segments at said output terminal.

12. The method of claim 1 in which generating first, second, third, and fourth filtered waveform segments comprises using the first, second, third, and fourth bit sequences respectively as an address to a look-up table containing one or more numerical samples of the first, second, third, and fourth filtered waveform segments.

13. The method of claim 12 in which the look-up table contains sigma-delta representations of the first, second, third, and fourth filtered waveform segments.

14. The method of claim 1 in which generating first, second, third, and fourth filtered waveform segments comprises outputting the first, second, third, and fourth bit sequences or their complements to a corresponding resistive combining network.

15. The method of claim 1 in which generating first, second, third, and fourth filtered waveform segments comprises outputting the first, second, third and fourth bit sequences and their complements to corresponding first and second complementary resistive combining networks to generate a balanced filtered waveform segment on two outputs corresponding to each of the first, second, third and fourth bit sequences.

16. The method of claim 15 in which combining filtered waveform segments corresponding to the first and third bit sequences comprises connecting the outputs of the corresponding resistive combining networks together.

17. The method of claim 16 in which the resistive combining networks corresponding to the first and third filtered waveforms have a relative impedance scaling to effect a predetermined weighted sum.

18. The method of claim 15 in which combining filtered waveform segments corresponding to the second and fourth bit sequences comprises connecting the outputs of the corresponding resistor networks together.

19. The method of claim 18 in which the resistive combining networks corresponding to the second and fourth filtered waveforms have a relative impedance scaling to effect a predetermined weighted sum.

20. The method of claim 1 in which the octal symbols are 8-PSK symbols.

21. A method for generating a modulation waveform for transmitting octal symbols, the modulation waveform comprising a real part and an imaginary part comprising:

inputting data symbols to a logic unit over a plurality of successive symbol periods, wherein each data symbol comprises a plurality of information bits:

forming in the logic unit at least two derived bits during each symbol period by combining selected information bits;

forming, during each symbol period, a plurality of bit sequences, each bit sequence containing bits input or derived over a plurality of symbol periods;

generating, during each symbol period, a plurality of filtered waveform segments using the bit sequences;

combining, during each symbol period, at least two of the filtered waveform segments to obtain a segment of the imaginary waveform part;

combining, during each symbol period, at least two of the filtered waveform segments to obtain a segment of the imaginary waveform part.

22. The method of claim 21 wherein the data symbol comprises first, second, and information bits.

23. The method of claim 22 in which the logic unit forms a first derived bit by an exclusive OR operation on first and third information bits.

24. The method of claim 22 in which the logic unit forms a second derived bit by an exclusive OR operation on second and third information bits and complementing the result.

25. The method of claim 21 in which the filtered waveform segments each comprise a number of numerical samples spaced over each symbol period.

26. The method of claim 21 in which the filtered waveform segments are represented by a sequence of sigma-delta values.

27. The method of claim 21 in which the modulation waveform is generated in balanced form on two outputs for each of the real and the imaginary parts.

28. The method of claim 27 in which the filtered waveform segments are produced as a balanced signal represented on two outputs and are represented by a sequence of sigma-delta values and its complement.

29. The method of claim 21 in which combining at least two of the filtered waveform segments to form a segment of the imaginary part of the modulation waveform comprises forming a weighted sum of a numerical sample of a first filtered waveform segment with a numerical sample of at least one other filtered waveform segment.

30. The method of claim 21 in which combining at least two of the filtered waveform segments to form a segment of the real part of the modulation waveform comprises forming a weighted sum of a numerical sample of a first filtered waveform segment with a numerical sample of at least one other filtered waveform segment.

31. The method of claim 21 in which combining at least two of the filtered waveform segments to form a segment of the imaginary part of the modulation waveform

comprises connecting a first filtered waveform segment through a first impedance to an output terminal and connecting a second filtered waveform segment through a second impedance to the output terminal to produce a weighted sum of the combined filtered waveform segments at the output terminal.

32. The method of claim 21 in which combining at least two of the filtered waveform segments to form a segment of the real part of the modulation waveform comprises connecting a first filtered waveform segment through a first impedance to an output terminal and connecting a second filtered waveform segment through a second impedance to the output terminal to produce a weighted sum of the combined filtered waveform segments at the output terminal.

33. The method of claim 21 in which generating a plurality of filtered waveform segments comprises using the bit sequences as an address to a look-up table containing pre-computed filtered numerical samples of the filtered waveform segments.

34. The method of claim 33 in which the look-up table contains oversampled sigma-delta representations of the pre-computed filtered waveform segments.

35. The method of claim 21 in which generating a plurality of filtered waveform segments includes inputting the bit sequences and their complements to a resistive combining network.

36. The method of claim 35 in which generating a plurality of filtered waveform segments comprises inputting the bit sequences and their complements to

corresponding first and second complementary resistive combining networks to generate balanced filtered waveform segments on two outputs corresponding to each of the bit sequences.

37. The method of claim 36 in which a first filtered waveform segment corresponds to a bit sequence comprising a plurality of first information bits, a second filtered waveform segment corresponds to a bit sequence comprising a plurality of second information bits, a third filtered waveform segment corresponds to a plurality of first derived bits, and a fourth filtered waveform segment corresponds to a plurality of second derived bits.

38. The method of claim 37 wherein the first filtered waveform segment is added to the third filtered waveform segment and the second waveform segment is added to the fourth filtered waveform segments by connecting the outputs of the corresponding resistive combining networks together.

39. The method of claim 38 in which the connected resistive combining networks have a relative impedance to effect a predetermined a weighted sum

40. The method of claim 21 in which the octal symbols are 8-PSK symbols.

41. A waveform generator for generating, from sequence of data symbol each having a plurality of information bits, a modulation waveform having a real part and an imaginary part, said waveform generator comprising:

a logic unit having an input for receiving said data symbols and an output,

wherein the logic unit combines, during each symbol period, selected

information bits comprising the data symbol to produce two or more derived bits, and wherein selected information bits and the derived bits are presented at the output of the logic unit;

a delay register connected to the output of the logic unit for storing a plurality of bit sequences, wherein each bit sequence comprises bits selected from the information bits and the derived bits over a plurality of symbol periods;

a filter generating a filtered waveform segment during each symbol period from the bit sequences;

a first combiner combining, during each symbol period, at least two of the filtered waveform segments to obtain a segment of the imaginary part of the modulation waveform; and

a second combiner combining, during each symbol period, at least two of the filtered waveform segments to obtain a segment of said real part of the modulation waveform.

42. The waveform generator of claim 41 wherein the filter comprises a look-up table storing waveform segment data corresponding to a plurality of filtered waveform segments, and wherein the waveform segment data is addressed by the bit sequences.

43. The waveform generator of claim 42 wherein the waveform segment data comprises a plurality of numerical values corresponding to samples of the filtered waveform segment spaced over the symbol period.

44. The waveform generator of claim 42 wherein the waveform segment data comprises a sequence of binary values using an oversampled sigma-delta representation.

45. The waveform generator of claim 44 wherein said first combiner comprises a two-wire resistive combining network for generating the real part of said waveform in balanced form from the sigma-delta representation of a first waveform segment, and the second combiner comprises a two-wire resistive combining network for generating the imaginary part of the waveform from the sigma-delta representation of a second waveform segment.

46. The waveform generator of claim 41 wherein the waveform generator includes first and second two-wire resistive combining networks for generating respectively the real and imaginary part of the modulation waveform in balanced form.

47. The waveform generator of claim 46 wherein the first combining network forms a weighted sum of first and second filtered waveform segments, and the second combining network forms a weighted sum of third and fourth filtered waveform segments.

48. The waveform generator of claim 46 wherein the bit sequences or their complements are output from the delay registers to respective resistive combining networks to form filtered waveform segments.

49. The waveform generator of claim 46 wherein the bit sequences and their complements are output from the delay registers to first and second complementary resistive combining networks to form balanced waveform segments on two wires.

50. The waveform generator of claim 41 including four delay registers for storing respectively sequences of a first information bit, a second information bit, a first derived bit, and a second derived bit over a predetermined number of symbol periods.

51. The waveform generator of claim 50 wherein the bit sequences stored in said first, second, third, and fourth registers are used to generate respectively a first waveform segment, a second waveform segment, a third waveform segment, and a fourth waveform segment.

52. The waveform generator of claim 51 wherein the first and third waveform segments are combined to generate the real part of the modulation waveform, and said second and fourth waveform segments are combined to form the imaginary part of the modulation waveform.

53. The waveform generator of claim 51 wherein the filter comprises a memory storing a plurality of waveform segments and wherein the bit sequences are used to address the memory.